

Abstract of the Disclosure:

A memory sense amplifier for a semiconductor memory device is provided with a compensation current source device that generates a compensation current and feeds it to an
5 interconnected bit line. The compensation current is selected in such a manner that during readout a potential gradient can be generated and/or maintained in cooperation with a compensation voltage source device on the selected and interlinked bit line device that is substantially constant
10 over time.

LDP/nt .